AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-9. (Canceled).

10. (Currently Amended) A packet switched backplane comprising

a backplane ~~that supports the PICMG 2.16 standard~~ including

a first node slot having a plurality of connectors including a first Ethernet connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a second node slot having a plurality of connectors including a second Ethernet connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets; and

a first aggregation slot having a plurality of single connectors including a third Ethernet connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a first dedicated link establishing a direct connection between the first and the third Ethernet connectors; and

a second dedicated link establishing a direct connection between the second and the third Ethernet connectors,

wherein the third Ethernet connector allows a first switch to turn on and off [[a]] data communication between the first Ethernet connector and the second Ethernet connector and via the first and second dedicated links.

11. (Currently Amended) The backplane according to claim 10, wherein ~~Ethernet transmit~~transmitting pins of the first and second Ethernet connectors are connected to ~~Ethernet receive~~receiving pins of the third Ethernet connector, and ~~Ethernet receive~~receiving pins of the first and second Ethernet connectors are connected to ~~Ethernet transmit~~transmitting pins of the third Ethernet connector.

12. (Currently Amended) The backplane according to claim 10, further comprising

a second aggregation slot having a plurality of connectors including a fourth Ethernet connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a third dedicated link establishing a direct connection between the first and the fourth Ethernet connectors; and

a fourth dedicated link establishing a direct connection between the second and the fourth Ethernet connectors,

wherein the fourth Ethernet connector allows a switch to turn on and off [[a]] data communication between the first Ethernet connector and the second Ethernet connector and via the third and fourth dedicated links.

13. (Canceled).

14. (Currently Amended) A data processing system comprising: ~~a packet switched backplane having~~

a packet switched backplane ~~that supports the PICMG 2.16 standard~~ including

a first node slot having a first single Ethernet ~~connector~~connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a second node slot having a second single Ethernet ~~connector~~connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a first aggregation slot having a third single Ethernet ~~connector~~connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets;

a first dedicated link establishing a direct connection between the first and the third single Ethernet connectors;

a second dedicated link establishing a direct connection between the second and the third single Ethernet connectors; and

a first aggregation card that is pluggable into the first aggregation slot including

a function unit that performs a ~~signal processing~~ main technical function in addition to Ethernet packet routing~~that is not associated with switching Ethernet packets~~; and

an Ethernet bridging unit that switches Ethernet packets,

wherein the third single Ethernet connector, when the first aggregation card is plugged into the first aggregation slot, allows the Ethernet bridging unit to turn on and

off [[a]] data communication that is between the first Ethernet connector and the second Ethernet connector and that is via the first and second dedicated links.

15. (Currently Amended) The data processing system according to claim 14 further comprising:

a first node card ~~that complies with the PICMG 2.16 standard and is~~ pluggable into the first node slot; and[[.]]

a second node card pluggable into the second node slot,

wherein, when the first node card, the second node card, and the first aggregation card are plugged into the first node slot, the second node slot, and the first aggregation slot respectively, the Ethernet bridging unit of the first aggregation card is coupled to the third single Ethernet connector and selectively switches Ethernet packets between the first node card and the second node card via the first and second dedicated links.

16. (Canceled).

17. (Currently Amended) The data processing system according to claim 15[[14]] further comprising:

~~at least one~~ a second aggregation slot ~~each~~ having a fourth single Ethernet connector ~~that complies with the PICMG 2.16 standard~~ for transferring and receiving Ethernet packets.

a third dedicated link establishing a direct connection between the first single Ethernet connector and the fourth single Ethernet connector; and

a fourth dedicated link establishing a direct connection between the second single Ethernet connector and the fourth single Ethernet connector.

18. (Currently Amended) The data processing system according to claim 17 further comprising ~~at least one~~ a second aggregation card that [[each]] is pluggable into ~~one of~~ the ~~at least one~~ second aggregation slot and that ~~each~~ includes

a function unit that performs a main technical function in addition to Ethernet packet routing~~signal processing function that is not switching Ethernet packets~~; and

an Ethernet bridging unit that switches Ethernet packets; ~~and is for communicating with one of the four Ethernet connectors.~~

wherein, when the first node card, the second node card, and the second aggregation card are plugged into the first node slot, the second node slot, and the second aggregation slot respectively, the Ethernet bridging unit of the second aggregation card is coupled to the fourth single Ethernet connector and selectively switches Ethernet packets between the first node card and the second node card via the third and fourth dedicated links.

19-20. (Canceled).

21. (Currently Amended) The data processing system according to claim 14, wherein ~~Ethernet transmit~~transmitting pins of the first and second single Ethernet connectors are connected to ~~Ethernet receive~~receiving pins of the third single Ethernet connector, and ~~Ethernet receive~~receiving pins of the first and second single Ethernet connectors are connected to ~~Ethernet transmit~~transmitting pins of the third single Ethernet connector.

22. (Currently Amended) The data processing system according to claim 14, wherein the Ethernet bridging unit of the first aggregation card is coupled to ~~further comprises~~ an external Ethernet connector connecting to an external address.

23. (Currently Amended) The data processing system according to claim [[22]]14 wherein the Ethernet bridging unit of the first aggregation card is an Ethernet switch.

24. (Currently Amended) A packet switched backplane comprising

a backplane employing a packet switched fabric including

a first node slot[[,]] having a plurality of single connectors including a first single Ethernet connector for transferring and receiving Ethernet packets~~, that complies with the requirements for a node slot in PICMG 2.16 standard~~;

a second node slot[[,]] having a plurality of single connectors including a second single Ethernet connector for transferring and receiving Ethernet packets~~, that complies with the requirements for a node slot in PICMG 2.16 standard~~; and

a first aggregation slot[[,]] that has[[ving]] a plurality of single connectors including a third single Ethernet connector for transferring and receiving Ethernet packets~~, that complies with the requirements for a node slot in PICMG 2.16 standard for selectively~~ and that receives[[ing]] ~~one from a source node card, a destination node card, and~~ an aggregation card, wherein the aggregation card ~~includes~~ is a node card equipped with an Ethernet bridging unit;

a first dedicated link establishing a direct point-to-point connection between the first and the third single Ethernet connectors; and

a second dedicated link establishing a direct point-to-point connection between the second and the third single Ethernet connectors,

wherein, when first, second node cards, and an aggregation card are plugged in the first, second node slots, and the first aggregation slot respectively, the Ethernet bridging unit of the aggregation card is coupled with the third single Ethernet connector and receives a packet from the first node card via the first dedicated link and further selectively transmits the received packet to the second node card via the second

dedicated link. ~~the third Ethernet connector allows a switch to turn on and off a communication between the first Ethernet connector and the second Ethernet connector and via the first and second dedicated links.~~

25. (Currently Amended) The packet switched backplane of claim 24, wherein the first dedicated link connects ~~Ethernet~~ transmitting pins of the first Ethernet connector ~~to Ethernet~~ with receiving[[e]] pins of the third single Ethernet connector, wherein the second dedicated link connects ~~Ethernet~~ receiving[[e]] pins of the second single Ethernet connector ~~to Ethernet~~ with transmitting pins of the third single Ethernet connector.

26. (New) The packet switched backplane of claim 1, wherein the plurality of connectors of each of the first node slot, the second node slot, and the first aggregation slot consist of five connector arranged in a column, the middle one of the five connectors in each column has transmitting and receiving pins,

wherein the first, second, and third Ethernet connectors are the middle one of the five connectors of the first node slot, the second node slot, and the first aggregation node slot, respectively.

27. (New) The packet switched backplane of claim 26, wherein the first dedicated link connects the transmitting pins of the first Ethernet connector with the receiving pins of the third Ethernet connector, wherein the second dedicated link

connects the receiving pins of the second Ethernet connector with the transmitting pins of the third Ethernet connector.